



***New Generation  
of  
Solid State Mass Memories***

- ① Introduction
- ① MdM NG –SEMM512
- ① Test bench
- ① State of development

## Introduction

- R&T CNES
- Take over from the Myriade Mass Memories
- Scientific Missions
- Needs:
  - Higher data rate (link with TMTHD)
  - Higher capacity
  - New interfaces (SpaceWire, TMTHD)
  - Drive by a remote computer
  - ITAR Free

# MM NG Presentation

## 🌀 Numbers:

- Capacity
  - 512Gbits (Flash EEPROM technology), organized by blocks
- Performances
  - 158Mbits/s Input and Output
- Consumption
  - Lower than 4W
- Dimensions
  - 220 x 115.5 x 22mm = Myriade
- Radiation tolerance
  - 20Krad (TBC)

# MM NG Presentation

## MM NG Vs MM Myriade

	MM Myriade	MM NG (SEMM512)
Capacity	8 Gbits (1 UPM) or 16 Gbits (2 UPM)	512 Gbits
Organisation mémoire	By blocks (1 block $\approx$ 32Ko)	By blocks (1 block $\approx$ 2.1Mo)
Input data rate	10Mbits/s	158 Mbits/s
Output data rate	16.8Mbits/s	158 Mbits/s
Consumption		4W max
Module size (mm)	220 x 115.5 x 22	220 x 115.5 x 22
Number of module	2 (UCM + 1 UPM) or 3 (UCM + 2 UPM)	1
Deficient blocks detection	Manually	Automatic

## Interfaces

- TM/TC
  - I2C, Oslink FdP, Oslink CU or UART (E2/S2/TMTC) , SpaceWire
- Input
  - High rate (E1 nominal and redundant), Oslink CU (E2), Oslink FdP, PacketWire FdP, SpaceWire
- Output
  - TMTHD (nominal and redundant), TMHD, Oslink CU (S2), Oslink FdP, SpaceWire

## Interfaces and performances

- I2C : 400KHz max
- Oslink FdP: 5, 10 or 20Mbits/s
- SpaceWire: (TBD)
- E1/E1P: Input High Rate: 158Mbits/s max
- E2/S2/TMTC: Oslink payload: 5, 10 or 20Mbits/s  
ou UART (TBD)
- PacketWire Motherboard: 40Mbits/s max
- TMTHD (nominal and redundant): 158Mbits/s
- TMHD: 89.6Mbits/s (max rate TMHD)

## Deficient blocks management

- The autotest is managed by TC from the computer
  - Autotest Reset
  - Autotest by profil 0xAA55
  - Autotest by profil 0x55AA
  - Autotest by profil shuffle

Write (or delete) following by a new read of the memory zone

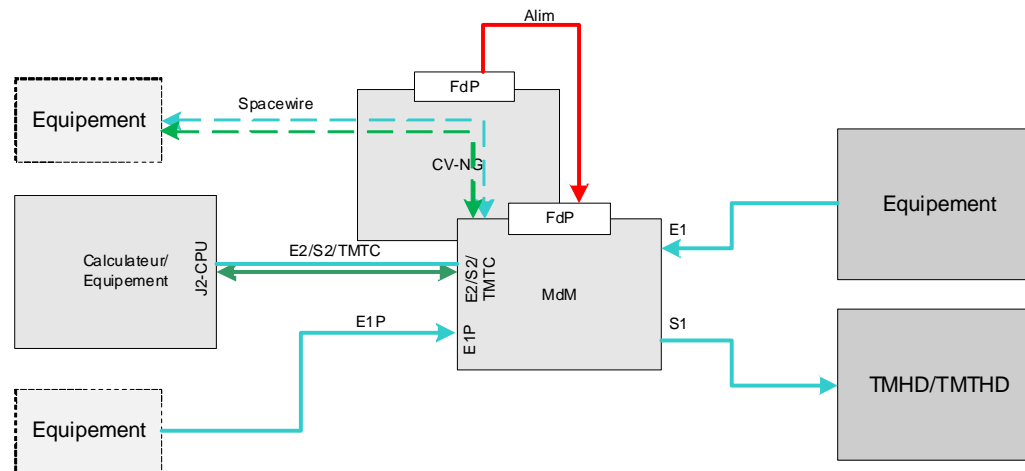
Data reading compare to the Date writing

- If at least 1 reading octet est different of 1 writing octet, the block is identified like deficient in a table inside the SRAM.
- Then several TC sent by the computer, allowed to the Mass Memory to take into account deficient blocks in the physical addressing.



# MM NG Presentation

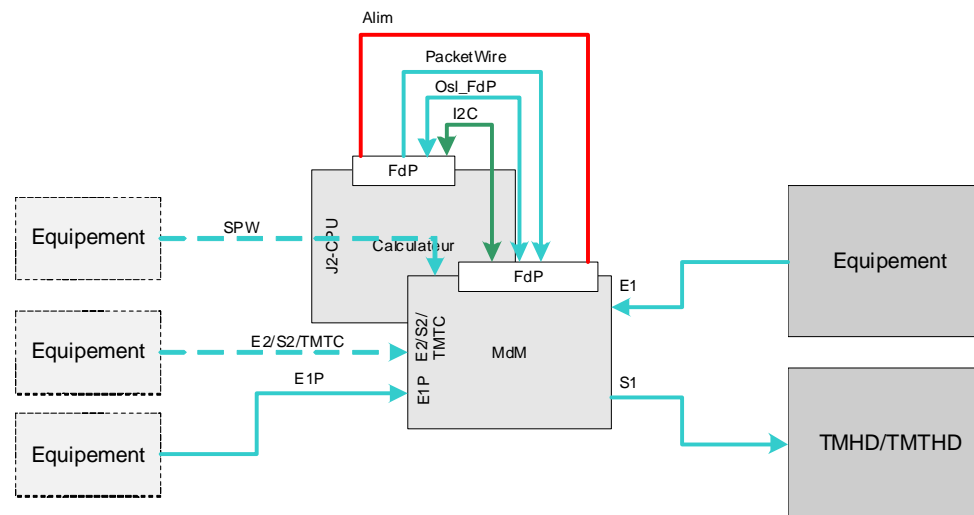
## Working Modes – Stand alone mode



- Power supply by converter through the motherboard
- Driving by a remote computer (through E2/S2/TMTC or SpaceWire)

# MM NG Presentation

## Working Modes – Integrated mode



- Driving by computer through the motherboard (lien I2C or Oslink FdP)

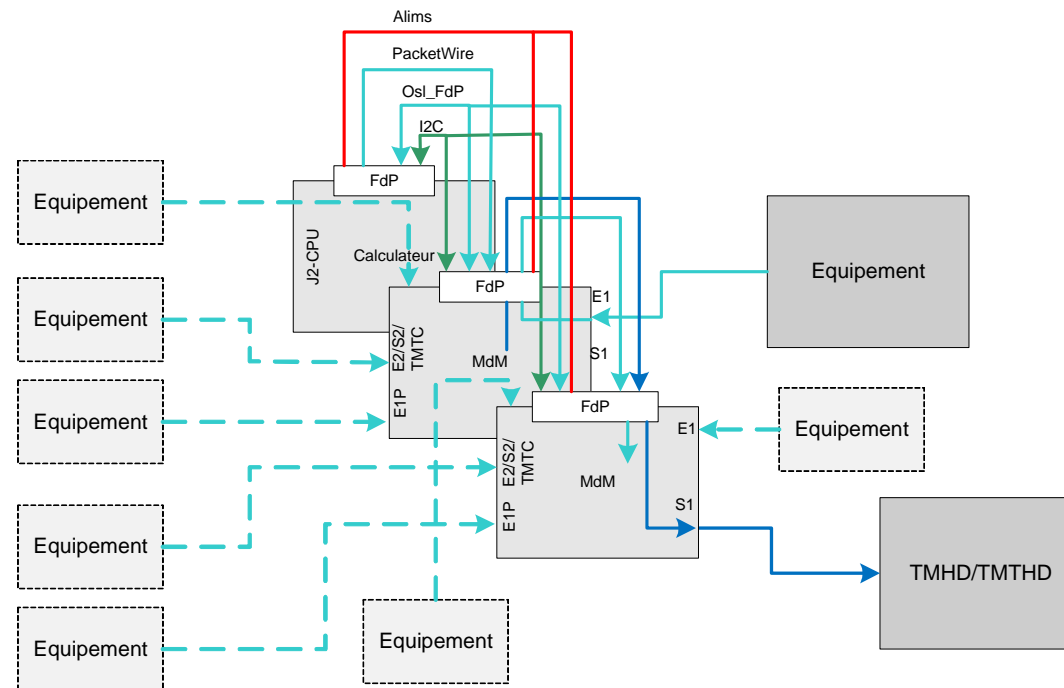
### Possibility to coupling 2 SEMM512

- By the motherboard
- Purpose:
  - Increase the storage capacity
  - Plug 2 payload equipments
  - Plug 2 TMHD or TMTHD

# MM NG Presentation

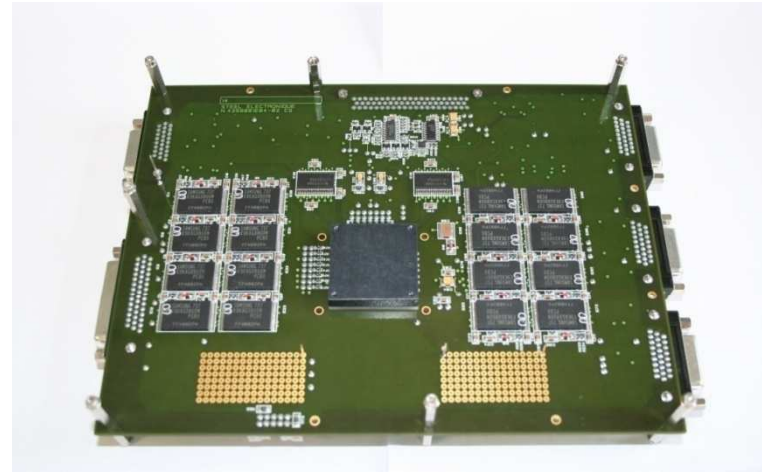
## ◉ Possibility to coupling 2 MM NG

- Exemple of 2 MM NG integrated in 1 OBC



## *State of developpement*

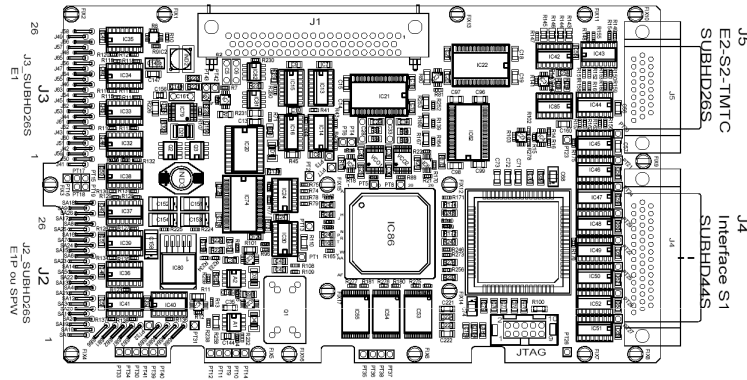
### 🔄 Evaluation MM NG model



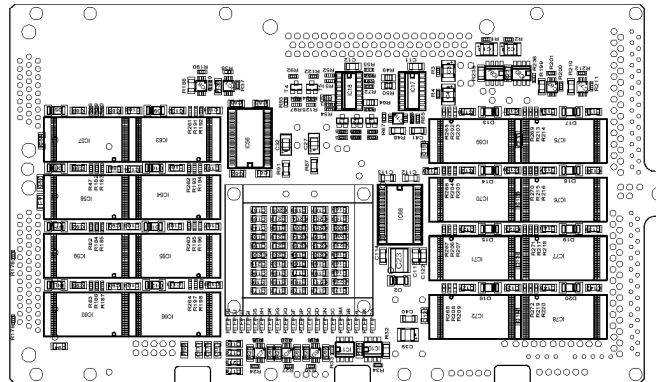
- Size higher to the flight board
- Ground components
- FPGA used: Actel ProASIC3E (A3PE1500)
- Links SpaceWire and UART not integrated in FPGA

# State of developpement

## Placement of the flight board



Components side:  
Fonction control/command



Soldering side:  
Memory

## *Test support presentation*

### 🌀 TM/TC Simulation:

- To several rates
- Sends TC, processing and storage of received TM
- Ability to process scripts (validation in progress)

### 🌀 Input Simulation

- To several rates
- Disponibility of several patterns (fix profil, incremented, file)

### 🌀 Output Simulation

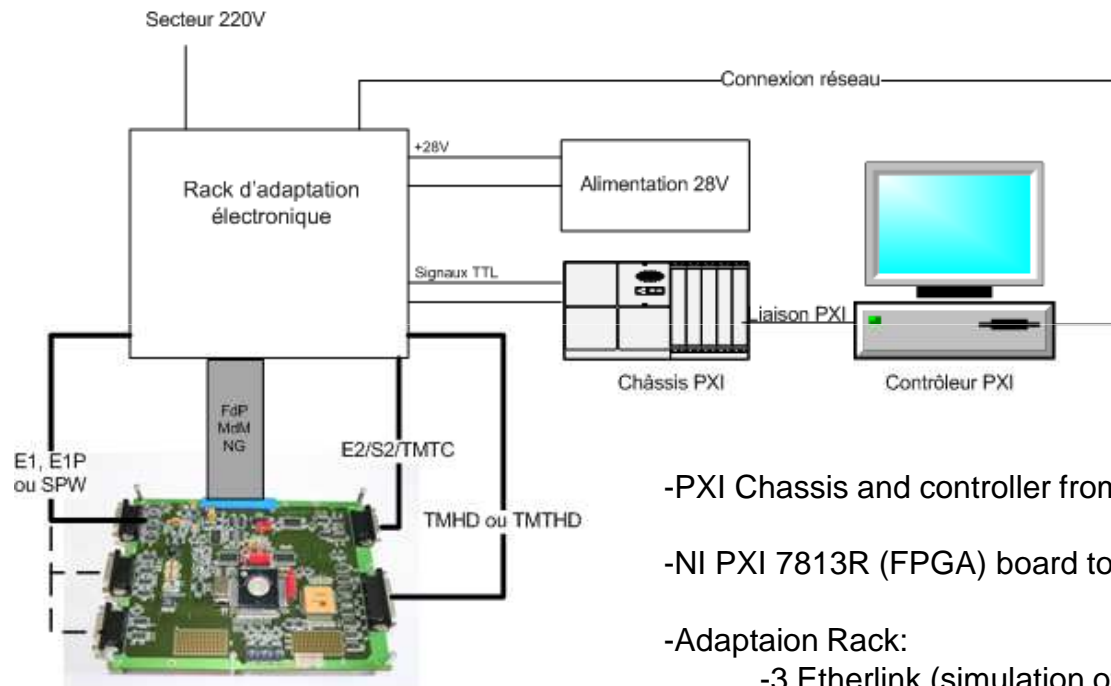
- To several rates
- Store reading data in files
- Controlling the flow of data read (channels TMHD and TMTHD)

### 🌀 Others utilities

- Binary files compare...

# Test Bench

## Hardware Architecture



-PXI Chassis and controller from NI (National Instruments)

-NI PXI 7813R (FPGA) board to manage high IF rates

-Adaptation Rack:

-3 Etherlink (simulation of Oslink links)

-1 module USB-I2C NI 8451

-3 electronics boards to generate voltage and signal adaptation



### Software Architecture

- Labview and Labview FPGA
  - To simulate high rates interfaces and manage the USB-I2C module
- LabWindows CVI
  - To drive Etherlink
  - HMI
  - Files managing
  - ...

# Test Bench

## Software Architecture : HMI

The screenshot displays the ETC MDM NG HMI interface, which is divided into several functional areas:

- TM/TC MM:** Located at the top left, it points to the 'TM-TC' section containing a list of commands such as 'TC\_ONOFF: Mise ON/OFF segment mémoire' and 'TC\_LECT\_TA: Lecture table d'anomalies'.
- Tasks execution Test bench:** Points to the 'Demande de Télémétries (uniquement pour I2C)' and 'Ordres ou TC Diverses' sections, which allow for sending specific test commands.
- TM/TC History:** Points to the 'Histo' section, which provides a log of executed commands and their results.
- MM feature:** Points to the 'Tableau de Bord' section, which displays the current configuration of the MDM, including 'Canal TMHD S1B', 'Canal TMHD S1A', and 'Horloge FdP: 10 MHz en entrée de la MDM'.
- Signal Control (from motherboard):** Points to the 'Interface E2/S2/IMTC' section, which includes controls for 'Reset E2', 'Fréq. 1Hz E2', and 'Mise à jour'.
- MM Status:** Points to the 'Mdm seule (Interface FdP)' section, which shows 'Fréq. 5/10MHz', 'Fréq. 1KHz', 'Fréq. 1Hz FdP', and 'Durée CMT\_Alim'.
- Test Bench Operation mode:** Points to the 'Etat de la MDM' section, which shows 'Mode de fonctionnement du banc' (Mode Manuel, Mode Script) and 'Etat de la MDM' (Mode, Table d'anomalies).

## *What's next ?*

### ① Product Space Industrialisation

- Design
  - Choice of Flight FPGA
  - Modification (SpaceWire, UART) and FPGA « Portage »
  - Grad 3 Components Upgrading
  - Mechanical design
  - Analysis (thermal, mechanical, reliability, FMECA)
  - Test Bench further design (SpaceWire, UART)
  
- EM Manufacturing (Myriade format)
  
- Test bench modification
  - Interfaces software modification (SpaceWire and UART)